

REMARKS/ARGUMENTS

Claims 1-23 are pending in the present application. The Examiner has rejected claims 1-23. Applicant respectfully requests reconsideration of pending claims 1-23.

The Examiner has objected to claim 15, alleging the following informalities: “claim recites the specific standard dimensions of the chassis that do not meet with the common claim language. Since the specification already disclosed the specific version and date of the standard dimensions, it is not necessary to recite it in the claim.” Applicant has amended claim 15 in accordance with the Examiner’s remarks. Applicant submits that such amendment is merely cosmetic in that it doesn’t alter the scope or meaning of the claim, but merely deletes language already present in the specification and deemed unnecessary in the claim by the Examiner. Thus, Applicant submits that claim 15 is in condition for allowance.

The Examiner has rejected claims 1-7, 12-14, 17-20, and 23 under 35 U.S.C. § 102(e) as being anticipated by Chong (U.S. Patent No. 6,434,221). Applicant respectfully disagrees.

Regarding claim 1, Applicant submits that the Examiner appears to attempt to characterize the “redundancy bus” of the cited reference as reading on a “metallic test access bus.” However, Applicant submits that the “redundancy bus” of the cited reference appears to be so named by virtue of its use to facilitate connection of a redundant xDSL modem card. Thus, Applicant submits that claim 1 is in condition for allowance.

Regarding claim 2, Applicant can find no disclosure of “a first portion...” and “a second portion...,” as recited in claim 2, in the portion of the cited reference cited by the Examiner. Thus, Applicant submits that the cited reference fails to anticipate the claimed invention as set forth in claim 2. Therefore, Applicant submits that claim 2 is in condition for allowance.

Regarding claim 3, as noted above regarding claim 1, Applicant submits that the “redundancy bus” of the cited reference appears to be so named by virtue of its use to facilitate connection of a redundant xDSL modem card. Thus, Applicant submits that claim 3 is in condition for allowance.

Regarding claim 4, as noted above regarding claim 1, Applicant submits that the “redundancy bus” of the cited reference appears to be so named by virtue of its use to facilitate connection of a redundant xDSL modem card. Thus, Applicant submits that claim 4 is in condition for allowance.

Regarding claim 5, in the portion of the cited reference cited by the Examiner, namely col. 3, lines 58-67, the CLT is described as performing tests to measure and/or determine one or more subscriber loop electrical characteristics, but not as “to provide stimulus over the at least one metallic test path.” Thus, Applicant submits that claim 5 is in condition for allowance.

Regarding claim 6, Applicant can find no reference in the portion of the cited referenced cited by the Examiner to “a control portion...” and a “stimulus portion...,” as recited in claim 6. Moreover, as noted in regard to claim 5, Applicant notes the CLT is described as performing tests to measure and/or determine one or more subscriber loop electrical characteristics, but not as “to convey stimulus...,” as recited in claim 6. Also, Applicant notes that the Examiner’s apparent citation of description of the CLT of the cited reference is inconsistent with the Examiner’s apparent citation of the “redundancy bus” of the cited reference as allegedly reading on the “metallic test access bus,” as it fails to show the cited reference as disclosing “wherein the metallic test access bus includes a control portion and a stimulus portion.” Thus, Applicant submits that the cited reference fails to anticipate the claimed invention. Therefore, Applicant submits that claim 6 is in condition for allowance.

Regarding claim 7, Applicant notes that the “conventional serial port” of col. 7, lines 26 and 27, of the cited reference refers to a direct CLT control port 552 completely separate and distinct from redundancy bus 186. Thus, Applicant submits that the cited reference fails to disclose a “metallic test access bus includes a control portion and a stimulus portion...,” “wherein the control portion of the metallic test access bus includes a serial data communication link.” Thus, Applicant submits that the cited reference fails to anticipate the claimed invention as set forth in claim 7. Therefore, Applicant submits that claim 7 is in condition for allowance.

Regarding claim 12, as noted above regarding claim 1, Applicant submits that the “redundancy bus” of the cited reference appears to be so named by virtue of its use to facilitate connection of a redundant xDSL modem card. Thus, Applicant submits that claim 12 is in condition for allowance.

Regarding claim 13, as noted above regarding claim 1, Applicant submits that the “redundancy bus” of the cited reference appears to be so named by virtue of its use to facilitate connection of a redundant xDSL modem card. Thus, Applicant submits that claim 13 is in condition for allowance.

Regarding claim 14, the Examiner cites Fig. 3 of the cited reference as teaching wherein the predetermined number of card slots is at least 12 card slots. However, Applicant does not see at least 12 card slots depicted in Fig. 3 of the cited reference. Thus, Applicant submits that the cited reference

fails to anticipate the claimed invention as set forth in claim 14. Therefore, Applicant submits that claim 14 is in condition for allowance.

Regarding claim 17, the Examiner asserts that claim 17 recites subject matter that is inherent in the teachings of the cited reference. However, Applicant submits that the teachings of the cited reference fail to establish inherency in accordance with existing law. For example, Applicant submits that the Examiner has failed to establish that the public gained the benefit of the subject matter recited in claim 17 from the teachings of the cited reference. *Schering Corp. v. Geneva Pharmaceuticals*, 339 F.3d 1373 (Fed. Cir. 2003). As another example, Applicant submits that the Examiner has failed to establish that the subject matter recited in claim 17 is present in the teachings of the cited reference. *Mentor v. Medical Device Alliance*, 244 F.3d 1365 (Fed. Cir. 2001); *Scaltech v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999). Thus, Applicant submits that the subject matter recited in claim 17 cannot be considered to be inherent in the teachings of the cited reference. Therefore, Applicant submits that the Examiner has not shown claim 17 to be anticipated by the cited reference. Consequently, Applicant submits that claim 17 is in condition for allowance.

Regarding claim 18, Applicant submits that the cited reference fails to disclose the claimed invention as set forth in claim 18. For example, Applicant submits that the cited reference fails to disclose "issuing control signals on a metallic test access bus included in a backplane of a chassis that includes a predetermined number of card slots, wherein each of the predetermined number of card slots has input/output ports, wherein the control signals operate to selectively couple the metallic test access bus to an input/output port of a first card slot to provide a first metallic test path." Rather, Fig. 5 of the cited reference shows that test and switching unit 130 of the cited reference does not provide for "issuing control signals on a metallic test access bus included in a backplane of a chassis...," "wherein the control signals operate to selectively couple the metallic test access bus to an input/output port of a first card...."

As another example, Applicant submits that the portion of the cited reference cited by the Examiner, namely col. 3, lines 58-67, fails to disclose "applying stimulus on the first metallic test path to produce a first response" and "measuring the first response," as recited in claim 18. Rather, col. 3, lines 58-60, merely state, "the CLT performs tests to measure and/or determine one or more subscriber loop electrical characteristics." Thus, Applicant submits that the cited reference fails to anticipate the claimed invention as set forth in claim 18. Therefore, Applicant submits that claim 18 is in condition for allowance.

Regarding claim 19, Applicant submits that the portion of the cited reference cited by the Examiner, namely col. 3, lines 26-43, states, specifically in col. 3, lines 32 and 33, "In response to a signal, command, or directive issued by the control unit, the relay matrix may route signals...." However, Applicant notes that col. 3, lines 26-28, state, "The test and switching unit...comprises...control logic, [and] a relay matrix...." Thus, Applicant submits that the "signal, command, or directive" described in col. 3, lines 32 and 33, appears to be internal to the "test and switching unit," and the cited reference apparently fails to disclose "issuing control signals on a metallic test access bus included in a backplane of a chassis...," "wherein issuing the control signals configures relays...." Thus, Applicant submits that the cited reference fails to anticipate the claimed invention as set forth in claim 19. Therefore, Applicant submits that claim 19 is in condition for allowance.

Regarding claim 20, the Examiner cites col. 10, lines 10-28, which describes the flowchart of Fig. 9, as teaching "wherein applying stimulus includes applying first stimulus on the first metallic test path to produce the first response and applying second stimulus on the second metallic test path to produce a second response, wherein measuring includes measuring the first and second responses." However, Applicant submits the teachings of Fig. 9 actually teach away from the present invention as set forth in claim 20. For example, Applicant notes that the arrow from step 916 returns the method to step 910 (col. 10, lines 51 and 52). If the Examiner is alleging that steps 900-906 of Fig. 9 read on "wherein the control signals operate to selectively couple the metallic test access bus to the input/output port of the first card slot to provide the first metallic test path," Applicant can find no teaching in the cited reference that steps 900-906 of Fig. 9 also teach "further operate to selectively couple the metallic test access bus to an input/output port of a second card slot to provide a second metallic test path," and submits that the arrow from step 916 to step 910 teaches away from iteratively performing steps 900-906 "to provide a second metallic test path." Moreover, Applicant submits that the "test and switching unit" of col. 3, lines 26-43 is not disclosed as providing an ability to establish multiple metallic test paths. Furthermore, Applicant notes, as stated in reference to claim 18 above, that the cited reference fails to disclose "issuing control signals on a metallic test access bus included in a backplane of a chassis that includes a predetermined number of card slots, wherein each of the predetermined number of card slots has input/output ports, wherein the control signals operate to selectively couple the metallic test access bus to an input/output port of a first card slot to provide a first metallic test path." Thus, Applicant submits that, even if the Examiner were alleging that steps 900-906 of Fig. 9 read on "wherein the control signals operate to selectively couple the metallic test

access bus to the input/output port of the first card slot to provide the first metallic test path," such an allegation would not be supported by the teachings of the cited reference. Also, as stated above in regard to claim 5, in the portion of the cited reference cited by the Examiner, namely col. 3, lines 58-67, the CLT is described as performing tests to measure and/or determine one or more subscriber loop electrical characteristics, but not as "applying stimulus on the first metallic test path to produce a first response." Thus, Applicant submits that the cited reference fails to render obvious the present invention as set forth in claim 20. Therefore, Applicant submits that claim 20 is in condition for allowance.

Regarding claim 23, the Examiner cites col. 7, lines 19-21, of the cited reference, which states, "Similarly, the control logic 520 is coupled to the control bus 184 via a second connector 504, and the relay matrix 530 is coupled to the redundancy bus 186 via a third connector 506." However, such teaching fails to disclose "wherein the control signals are issued over a control portion of the metallic test access bus..." and "...wherein the control signals operate to selectively couple the metallic test access bus to an input/output port of a first card slot to provide a first metallic test path," as recited in claim 23, as the cited reference does not appear to disclose any control signals being issued over control bus 184 "wherein the control signals operate to selectively couple the metallic test access bus to an input/output port of a first card slot to provide a first metallic test path." Thus, Applicant submits that the cited reference fails to anticipate the present invention as set forth in claim 23. Therefore, Applicant submits that claim 23 is in condition for allowance.

The Examiner has rejected claims 8-11, 15, 16, 21, and 22 under 35 U.S.C. § 103(a) as being unpatentable over Chong (U.S. Patent No. 6,434,221). Applicant respectfully disagrees.

Regarding claim 8, the Examiner acknowledges that Chong did not clearly suggest wherein the stimulus portion of the metallic test access bus includes at least six conductor pairs, but alleges that it is obvious to one of the ordinary skill in the art since the numbers of conductor pairs are based on the standard configuration of the particular system. Applicant submits that, by stating "is obvious" in the present tense, the Examiner is improperly rejecting claim 8 based on what the Examiner alleges would be obvious to one of ordinary skill in the art at the time the Examiner issued the rejection, not at the time the invention was made. Moreover, Applicant submits that the Examiner does not identify what the Examiner considers to be "the standard configuration of the particular system." Applicant notes that claim 8 does not recite "the standard configuration of the particular system." Thus, Applicant

submits that claim 8 is not rendered obvious by the cited reference. Therefore, Applicant submits that claim 8 is in condition for allowance.

Regarding claim 9, the Examiner acknowledges that Chong did not clearly suggest wherein the stimulus portion of the metallic test access bus includes at least six conductor pairs, but alleges that it is obvious to one of the ordinary skill in the art since the numbers of conductor pairs are based on the standard configuration of the particular system. Applicant submits that, by stating "is obvious" in the present tense, the Examiner is improperly rejecting claim 9 based on what the Examiner alleges would be obvious to one of ordinary skill in the art at the time the Examiner issued the rejection, not at the time the invention was made. Moreover, Applicant submits that the Examiner does not identify what the Examiner considers to be "the standard configuration of the particular system." Applicant notes that claim 9 does not recite "the standard configuration of the particular system." Thus, Applicant submits that claim 9 is not rendered obvious by the cited reference. Therefore, Applicant submits that claim 9 is in condition for allowance.

Regarding claim 10, the Examiner acknowledges that the cited reference did not clearly suggest wherein the stimulus conveyed includes at least one of a Safety Extra Low Voltage (SELV) rated stimulus and a Telecom Network Voltage (TNV) rated stimulus, but states that the Examiner takes official notice that it is well known in the art and concludes that "it would be obvious to one of the ordinary to recognize such test signals are need in order to test both the DSL and conventional circuit." However, Applicant submits that the Examiner fails to identify what "it" is of which official notice is purportedly taken and how such purported official notice could lead to the Examiner's conclusion. Applicant submits that, by stating "is obvious" in the present tense, the Examiner is improperly rejecting claim 10 based on what the Examiner alleges would be obvious to one of ordinary skill in the art at the time the Examiner issued the rejection, not at the time the invention was made. Also, Applicant submits that the Examiner does not define what the Examiner describes as a "conventional circuit," nor how such circuit would relate to the claimed subject matter. Thus, Applicant submits that the Examiner has not established a *prima facie* showing of obviousness with respect to claim 10. Therefore, Applicant submits that claim 10 is in condition for allowance.

Regarding claim 11, the Examiner states, "As suggested above, Chong teaches wherein in a first configuration the metallic test access bus is operable to couple an input/output port of a first card slot and an input/output port of a second card slot, wherein the metallic test access bus is operable to convey the SELV rated stimulus to the input/output port of the first card slot and to convey the TNV

rated stimulus to the input/output port of the second card slot,” citing col. 3, lines 44-67. However, Applicant notes that the Examiner does not appear to have “suggested above” that the cited reference includes such teaching. In fact, in the context of the § 103(a) rejection, the Examiner has stated that the cited reference does not clearly suggest the features of the claims so rejected. Moreover, with regard to a SELV rated stimulus and a TNV rated stimulus, the Examiner purported to take official notice that “it” is well known in the art, but fails to identify what “it” is of which official notice is purportedly taken and how such purported official notice could lead to the Examiner’s conclusion. Also, Applicant submits that the Examiner does not define what the Examiner describes as a “conventional circuit,” nor how such circuit would relate to the claimed subject matter. As Applicant discloses on page 8, lines 9-11, of the specification (and submits the cited reference fails to disclose), “Supporting such a variety of signaling levels presents additional challenges for integrated multi-services access platforms, and techniques for addressing such concerns are described in additional detail below.” Thus, Applicant submits that mere awareness of TNV levels and SELV levels would not render obvious the subject matter of claim 11, but rather, in view of the teachings of the cited reference, teaches away from the claimed invention as set forth in claim 11. Thus, Applicant submits that claim 11 is in condition for allowance.

Regarding claim 15, the Examiner acknowledges that the cited reference did not clearly suggest wherein dimensions of the chassis are each within three inches of standard dimensions but purports to take official notice that it is well known in the art. Applicant notes that the Examiner fails to identify what “it” is of which official notice is purportedly taken and how such purported official notice could lead to the Examiner’s conclusion. Also, as above, Applicant submits that the Examiner does not explain why the Examiner asserts that “it would have been obvious to one of the ordinary skill in the art at the time the invention was made to recognize that a particular chassis must be within certain dimension in order to comply with the standard requirement,” yet offers no showing that the prior art teaches “a particular chassis must be within certain dimension in order to comply with the standard requirement.” Thus, Applicant submits that the Examiner has not established a *prima facie* showing of obviousness with respect to claim 15. Therefore, Applicant submits that claim 15 is in condition for allowance.

Regarding claim 16, the Examiner acknowledges that the cited reference did not clearly suggest wherein dimensions of the chassis are not greater than approximately 18 inches wide, 22 inches tall, and 12 inches deep and purports to assert official notice that it is well known in the art.. Applicant

notes that the Examiner fails to identify what “it” is of which official notice is purportedly taken and how such purported official notice could lead to the Examiner’s conclusion. Also, as above, Applicant submits that the Examiner does not explain why the Examiner asserts that “it would have been obvious to one of the ordinary skill in the art at the time the invention was made to recognize that a particular chassis must be within certain dimension in order to comply with the standard requirement,” yet offers no showing that the prior art teaches “a particular chassis must be within certain dimension in order to comply with the standard requirement.” Thus, Applicant submits that the Examiner has not established a *prima facie* showing of obviousness with respect to claim 16. Therefore, Applicant submits that claim 16 is in condition for allowance.

Regarding claim 21, the Examiner purports to take official notice that “it” is well known in the art and concludes that “it would be obvious to one of the ordinary to recognize that such test signals are need in order to test both the DSL and conventional circuit.” However, Applicant submits that the Examiner fails to identify what “it” is of which official notice is purportedly taken and how such purported official notice could lead to the Examiner’s conclusion. Also, Applicant submits that the Examiner does not define what the Examiner describes as a “conventional circuit,” nor how such circuit would relate to the claimed subject matter. As Applicant discloses on page 8, lines 9-11, of the specification (and submits the cited reference fails to disclose), “Supporting such a variety of signaling levels presents additional challenges for integrated multi-services access platforms, and techniques for addressing such concerns are described in additional detail below.” Thus, Applicant submits that mere awareness of TNV levels and SELV levels would not render obvious the subject matter of claim 21, but rather, in view of the teachings of the cited reference, teaches away from the claimed invention as set forth in claim 21. Thus, Applicant submits that claim 21 is in condition for allowance.

Regarding claim 22, as with claim 21, Applicant notes that the Examiner fails to identify what “it” is of which official notice is purportedly taken and how such purported official notice could lead to the Examiner’s conclusion. Also, as above, Applicant submits that the Examiner does not define what the Examiner describes as a “conventional circuit,” nor how such circuit would relate to the claimed subject matter. Thus, Applicant submits that the Examiner has not established a *prima facie* showing of obviousness with respect to claim 22. Therefore, Applicant submits that claim 22 is in condition for allowance.

In conclusion, Applicant has overcome all of the Office’s rejections, and early notice of allowance to this effect is earnestly solicited. If, for any reason, the Office is unable to allow the

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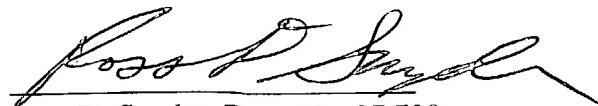
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Application on the next Office Action, and believes a telephone interview would be helpful, the Examiner is respectfully requested to contact the undersigned attorney.

Respectfully submitted,

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Date



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